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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,187	12/22/2004	Satoshi Funada	0670-7051	6815

31780 7590 02/22/2008

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EXAMINER	
NOONAN, WILLOW W	
ART UNIT	PAPER NUMBER
2146	

MAIL DATE	DELIVERY MODE
02/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/519,187	FUNADA, SATOSHI	
	Examiner	Art Unit	
	WILLOW NOONAN	2146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/12/2005, 12/22/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/814,821 has a total of 14 claims pending in the application; there are 6 independent claims and 8 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Priority

3. As required by M.P.E.P. 201.14(c), acknowledgement is made of applicant's claim for priority based on applications filed on June 26, 2002 (Japan 2002-186478).

Drawings

4. The applicant's drawings submitted are acceptable for examination purposes.

Information Disclosure Statement

5. As required by M.P.E.P. 609(C), the applicant's submissions of the Information Disclosure Statements dated September 12, 2005 and December 22, 2004 are acknowledged by the examiner and the cited references have been considered in the

examination of the claims now pending. As required by M.P.E.P 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1-2, the phrase "to/from" renders the claims indefinite.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Rompaey (U.S. Patent No. 5,870,588).

Regarding claim 1, Rompaey teaches a hardware-implemented information processing apparatus comprising a plurality of processing circuit modules, each performing specific information processing in response to input of information data. *See* Rompaey at col. 6, lines 57-70 (“In another aspect of the present invention, the aspects

comprise any one or more of functional, communication, concurrency and structural aspects of the digital system. The objects representing the functional aspects comprise any one or more of host language encapsulations, threads, and context"); a merging circuit module that merges information data from a plurality of paths into one path, *see* Rompaey at col. 6, lines 18-34 (describing how hierarchal objects combine primitive components); and transmission means for performing one-way transmission of the information data in a data set form to/from the processing circuit modules, to/from the merging circuit module, and between the processing circuit modules and the merging circuit module. *See* Rompaey at fig. 10.

Regarding claim 2, Rompaey teaches a hardware-implemented information processing apparatus comprising one or more processing circuit modules and zero or one or more merging circuit modules, wherein the processing circuit modules and the merging circuit modules perform one-way information transmission of data sets containing certain information to/from the processing circuit modules, the merging circuit modules, or an I/O interface; wherein each of the processing circuit modules has a circuit for performing a function specific to the module and has zero or one input and zero or more outputs; and wherein each of the merging circuit modules has two or more inputs and one output and merges output data sets from two or more circuits into one output. *See* Rompaey at fig. 10; Rompaey at col. 7, paragraph 1.

Regarding claim 3, Rompaey teaches an information processing apparatus comprising: a plurality of hardware modules, each configured by implementing one of functional units of certain information processing software as hardware; and

transmission means for performing one-way transmission of data between the hardware modules on a data set basis. *See* Rompaey at col. 7, paragraph 1.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey in view of Kay (U.S. Patent No. 6,021,266).

Regarding claim 4, Kay teaches that each functional unit of the software corresponds to a software component in which header and data information is communicated and processing is performed by, for example, a function call in C language. *See* Kay at fig. 1. It would have been obvious to one of ordinary skill to use Kay's technique with Rompaey's system because both disclose similar systems and methods for designing and implementing hardware integrated circuits. *See* Kay, *Abstract*.

Regarding claims 5 and 6, Examiner takes official notice that functionality for an internet server and for data mining, natural language processing, network information processing, DNA computation and simulation, physical simulation, and audio/video processing are well known in the art.

Regarding claims 7, 12, and 14, Rompaey teaches a method of manufacturing an information processing apparatus, the method comprising the steps of:

dividing a software program that implements a certain information processing function on a general- purpose computer into one or more arbitrary functional units, *see* Rompaey at col. 6, lines 57-70 ("In another aspect of the present invention, the aspects comprise any one or more of functional, communication, concurrency and structural aspects of the digital system. The objects representing the functional aspects comprise any one or more of host language encapsulations, threads, and context");

providing a hardware-implemented processing circuit module that has zero or one input and zero or one or more outputs communicating the functional units via data sets of an arbitrarily fixed or variable length, and operates based on the data sets to perform certain processing corresponding to one of the functional units provided by dividing, *see* Rompaey at fig. 10; and

providing a hardware-implemented merging circuit module that has a plurality of inputs and one output and operates to merge inputs of the data sets from the inputs into one output; wherein one or more of the processing circuit modules are combined with each other and optionally the inputs and the output of one or more of the merging circuit modules are further combined therewith so that processing operation implemented by the software program and the general-purpose computer is implemented by hardware circuits, *see* Rompaey at col. 6, lines 18-34 (describing how hierarchal objects combine primitive components); Kay at fig. 2 (#16).

Regarding claim 8, Kay teaches that the processing circuit module is configured as a gate array. *See* Kay at col. 1, lines 14-20.

Regarding claim 9, Rompaey teaches that the data set includes a header section and a data section, the header section containing information for the processing circuit module to control another processing circuit module connected directly or indirectly thereto. *See* Rompaey at p. 13, paragraph 3 ("A protocol may further have an index set. The indices in the index set are used to convey extra information about the data that is transported. For example the primitive protocol used to model the memory port of a processor will have an index to model the address of the data that is put on the memory port").

Regarding claim 10, Rompaey teaches that the merging circuit module includes a storage device for 15 temporarily storing the input data sets. *See* Rompaey at col. 14, lines 65-67 ("FIFO hierarchical channel (44) takes care of the necessary buffering of data").

Regarding claim 11, Kay teaches that the processing circuit module and the merging circuit module include means for feeding back a processing state of the input data sets. *See* Kay at col. 12, paragraph 2 ("Because each computation may take an unknown time to complete, for instance if it sends or receives from a channel or external device, performs a data dependent calculation, or performs a function call, the circuit performing the computation must be able to signal its completion and wait until its value has been used before disasserting it").

Regarding claim 13, teaches that in the step of combining the processing circuit modules and optionally the merging circuit module with the software part, the functional units to be replaced in the software program are replaced one by one with the processing circuit modules or the merging circuit module while being verified for operation. *See* Rompaey at col. 23, lines 51-56 ("After the partitioning of the system has been verified by simulation and before the actual implementation takes place, the designer may choose to refine the communication mechanism between the processors").

Conclusion

12. Please see the included *Notice of References Cited* for additional prior art considered pertinent to applicant's disclosure but not explicitly relied upon in this action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Willow Noonan whose telephone number is (571) 270-1322. The examiner can normally be reached on Monday through Friday, 7:30 AM-5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Pwu can be reached on (571) 272-6798. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Willow Noonan/

Examiner, Art Unit 2146

/Jeffrey C Pwu/

Supervisory Patent Examiner, Art Unit 2146